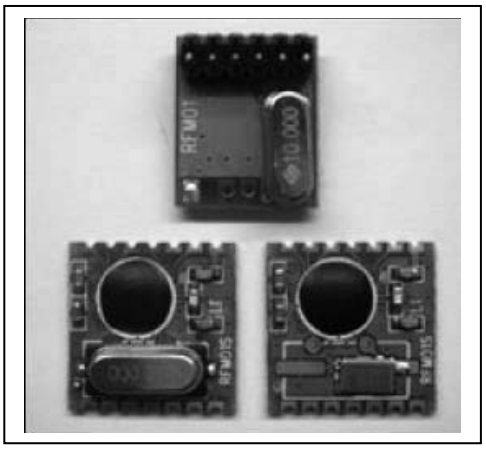
ISM BAND FSK EMPFANGSMODUL

RFM01

RFM01 ist ein kostengünstiges ISM-Band-Empfangsmodul. Es arbeitet mit FSK-Modulation im 433 MHZ Band.
Über die integrierte SPI-Schnittstelle kann das RFM01-Modul komfortabel von einem Microcontroller programmiert und konfiguriert werden.



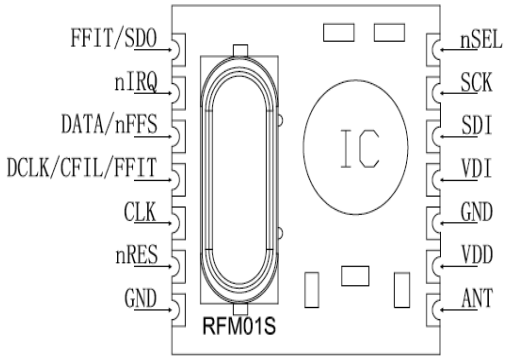
Features:

- Hervorrangendes Preis/Leistungsverhältnis
- keine Abstimmung notwendig
- FSK-Empfang
- PLL und Zero-IF Technologie
- Schnelle PLL-Abstimmzeit
- Hochauflösende PLL mit 2.5 KHz Schritten
- Hohe Datenrate (bis zu 115.2 kbps mit internen Demodulator, mit externen RC-Filter Datenrate bis zu 256 kbps)
- Differential-Antennen-Eingang
- Automatische Antennenabstimmung
- Programmierbare Empfänger-Bandbreite (von 67 bis 400 kHz)
- Analoge und digitale Signal-Stärke-Auswertung (ARSSI/DRSSI)
- AFC
- DQD
- Interner Demodulator
- SPI-Schnittstelle
- Clock- und Reset-Signal Ausgang für externen Mikrokontroller
- 16 Bit FIFO
- Low-Power-Modus (<0.5mA durchschnittliche Stromaufnahme)
- 10MHz Quarz für PLL-Timing
- Wakeup-Timer
- Low-Battery Erkennung
- Programmierbare Kapazitäten
- 2.2...5.4V- Betriebsspannung
- Niedrige Stromaufnahme
- StandBy-Stromaufnahme niedriger als 0.3uA

Typische Anwendungen：

- Fernbedienungsempfänger
- Schnurlose Datenübertragung
- Sichrheitssysteme
- Spielzeug
- Reifenluftdruck-Monitoring-System

Pin-Belegung：



Bezeichnung	Typ	Funktion
VDI	DO	Valid data indicator
VDD	S	Positive power supply
SDI	DI	SPI data input
SCK	DI	SPI clock input
nSEL	DI	Chip select (active low)
FFIT/SDO	DO	FIFO fill interrupt(active low) or status read data output
nRES	DO	Reset output（active low）
GND	S	Power ground
nIRQ	DO	Interrupts request output（active low）
DATA/nFFS	DO/DI	Data input(non FIFO mode)/ FIFO select
DCLK/CFIL/FFIT	DO/AIO/DO	Clock output (no FIFO)/ external filter capacitor(analog mode)/ FIFO interrupts(active high)when FIFO level set to 1, FIFO empty interruption can be achieved
CLK	DO	Clock output for external microcontroller

Electrical Parameter：

Maximum（not at working mode）

symbol	parameter	minimum	maximum	Unit
V_{dd}	Positive power supply	-0.5	6.0	V
V_{in}	All pin input level	-0.5	Vdd+0.5	V
I_{in}	Input current except power	-25	25	MA
ESD	Human body model		1000	V
T_{st}	Storage temperature	-55	125	℃
T_{ld}	Soldering temperature(10s)		260	℃

Recommended working range

symbol	parameter	minimum	maximum	Unit
V_{dd}	Positive power supply	2.2	5.4	V
T_{op}	Working temperature	-40	85	℃

DC characteristic

symbol	parameter	Remark	minimum	typical	maximum	Unit
I_{dd}	Current consumption	433MHz band		9	11	mA
I_x	Stand by current	Crystal and base band on		3．0	3．5	mA
I_{pd}	Sleep mode current	All blocks off		0.3		uA
I_{lb}	Low battery detection			0.5		uA
V_{lb}	Low battery step	0.1V per step	2.2		5.3	V
V_{lba}	Low battery detection accuracy			75		mV
V_{il}	Low level input				$0.3*V_{dd}$	V
V_{ih}	High level input		$0.7*V_{dd}$			V
I_{il}	Leakage current	V_{il}=0V	-1		1	uA
I_{ih}	Leakage current	$V_{ih}=V_{dd}$,V_{dd}=5.4V	-1		1	uA
V_{ol}	Low level output	I_{ol}=2mA			0.4	V
V_{oh}	High level output	I_{oh}=-2mA	V_{dd}-0.4			V

AC characteristic

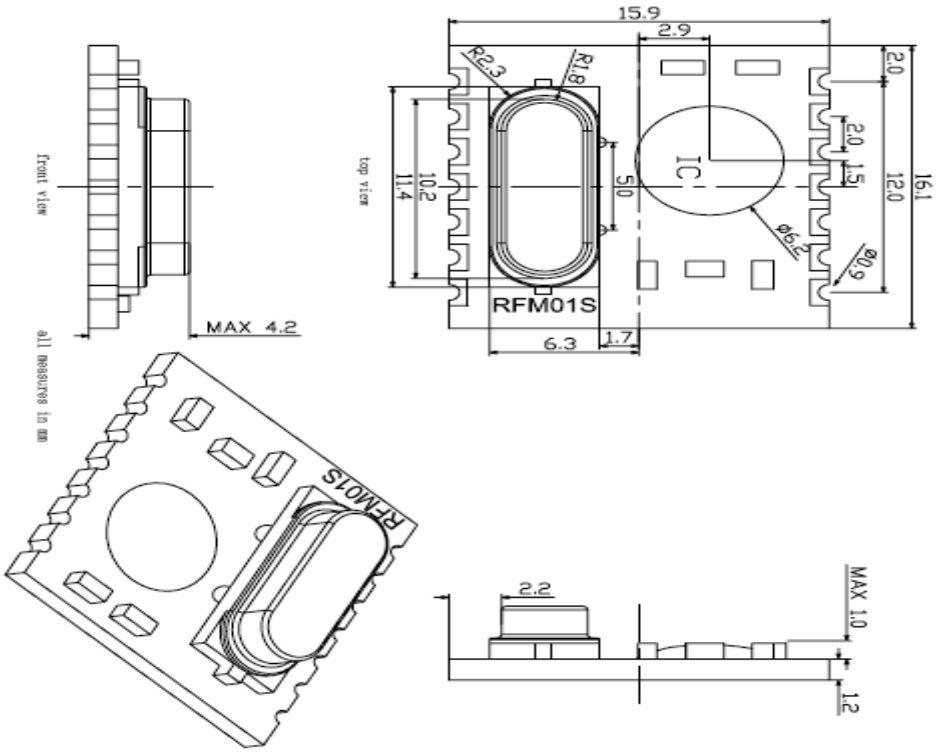
symbol	parameter	remark	min	typical	max	Unit
f_{ref}	PLL frequency	Parallel fundamental	8	10	12	MHz
f_{LO}	frequency (10MHz crystal used)	433 MHz band,2.5KHz step	430.24		439.75	MHz

BW	Receiver bandwidth	1 2 3 4 5 6	60 120 180 240 300 360	67 134 200 270 350 400	75 150 225 300 375 450	kHz
t_{lock}	PLL lock time	After 10MHz step hopping, frequency error <10 kHz		20		us
$T_{st, p}$	PLL start time	After crystal stabilized		250		us
BR	Data rate	With internal digital demodulator			115.2	kbps
BRA	Data rate	With external RC filter			256	kbps
P_{min}	sensitivity	BW=134KHz,BR=1.2kbps		-109	-100	dBm
AFC_{range}	AFC working range	∂ F_{fsk}: received signal modulation depth		0.8*∂ F_{fsk}		
RS_A	RSSI accuracy			±5		dB
RS_R	RSSI range			46		dB
C_{ARSSI}	ARSSI filter			1		nF
RS_{STEP}	RSSI programmable step			6		dB
RS_{RESP}	DRSSI response time	RSSI output high after valid , C_{ARRSI}=5nF		500		us
C_{XL}	Capacitor bank	Programmable step with 0.5pF step, +/- 10%	8.5		16	pF
T_{POR}	PWR time	V_{dd} reach 90%		50	100	mS
T_{PBT}	Wakeup timer period	Calibrated each 30s	0．96		1．08	mS
$T_{WAKE-UP}$	Programmable wakeup time		1		5*10E11	mS
T_{SX}	Crystal start up time	Crystal ESR < 100 Ohms			5	mS
$C_{IN,D}$	Load capacitance				2	pF
$T_{r,F}$	Output rising edge	With 15PF load			10	ns

Mechanical Dimension

（units in mm）

SMD PACKAGE（S1）



Module Model Definition

model=module-operation band

RFM01-433-D/S

module type　　operation band　　Package

Note: SOP packages is divided into two kinds based on thickness: 1. thickness is 4.2mm, 2. thickness is 2.2mm

example：1，RFM01 module at 433MHz band ,SMD: RFM01-433-S。

RF01 programming guide

1. Brief description

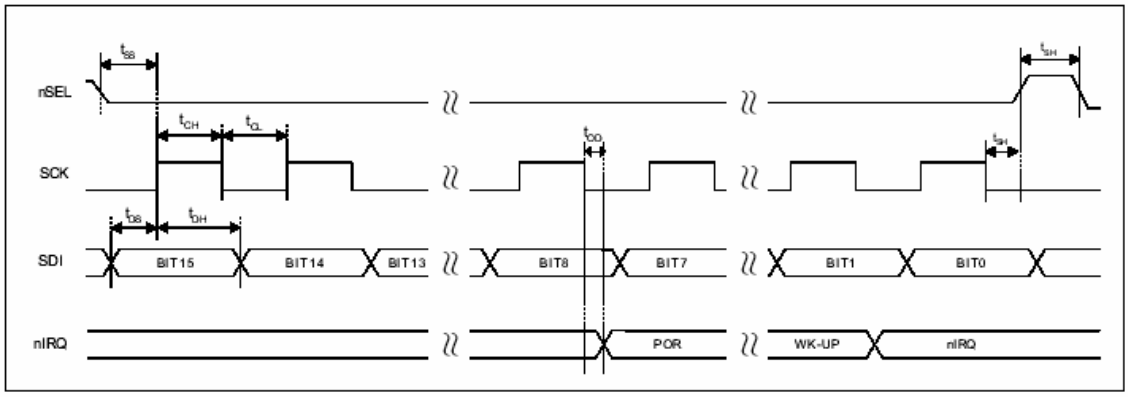
RF01 is a low cost FSK receive IC witch integrated all RF functions in a single chip. It only need a MCU, a crystal, a decouple capacitor and antenna to build a hi reliable FSK receiver .

RF01 supports a command interface to setup frequency, deviation, output power and also data rate. No need any hardware adjustment when using in frequency-hopping applications

RF01 can be used in applications such as remote control toys, w ireless alarm, wireless sensor, wireless keyboard/mouse, home-automation and wireless data collection.

2. Commands

1. Timing diagram



2. Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	1	eb	et	ex	x3	x2	x1	x0	i2	i1	i0	dc	893Ah

eb：Enable low battery detection function

et：Enable wake-up timer

ex：Enable crystal oscillator

x3..x0: select crystal load capacitor

x3	x2	x1	x0	load capacitor [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
……		……		
1	1	1	0	15.5
1	1	1	1	16.0

i2..i0:select baseband bandwidth

i2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved

dc：Disable signal output of CLK pin

3. Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

f11..f0: Set operation frequency

433band: Fc=430+F*0.0025 MHz

Fc is carrier frequency, F is frequency parameter and 36⩽ F⩽ 3903

4. Receiver Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d1	d0	g1	g0	r2	r1	r0	en	C0C1h

d1..d0: select VDI source

d1	d0	VDI output
0	0	Digital RSSI output(DRSSI)
0	1	Data quality detection output (DQD)
1	0	Clock recovery lock output
1	1	Always on

g1..g0: select LNA gain

g1	g0	LNA gain (dBm)
0	0	0
0	1	-14
1	0	-6
1	1	-20

r2..r0: select DRSSI threshold

r2	r1	r0	RSSIsetth [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	-67
1	0	1	-61

The actual DRSSI threshold is related to LNA setup:

$$RSSI_{th} = RSSI_{setth} + G_{LNA.}$$

en: Enable the receiver

5. Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up period is determined by:

$$T_{wake\text{-}up} = M * 2^{R} [ms]$$

For continual operation, bit 'et' must be cleared and set

6. Low Duty-Cycle Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	d6	d5	d4	d3	d2	d1	d0	en	CCOEh

d6..d0: Set duty cycle

D.C.= (D * 2 +1) / M *100%

en：Enable low duty cycle mode

7. Low Battery Detector and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	d2	d1	d0	t4	t3	t2	t1	t0	C200h

d2..d0: select frequency of CLK pin

d2	d1	d0	Clock frequency[MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

CLK signal is derive form crystal oscillator and it can be applied to MCU clock in to save a second crystal.

If not used, please set bit "dc" to disable CLK output

To integrate the load capacitor internal can not only save cost, but also adjust reference frequency by software

t4..t0: Set threshold voltage of Low battery detector：

Vlb=2.2+T*0.1 [V]

8. AFC Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	a1	a0	rl1	rl0	st	fi	oe	en	C6F7h

a1..a0: select AFC auto-mode：

a1	a0	
0	0	Controlled by MCU
0	1	Run once at power on
1	0	Keep offset when VDI hi
1	1	Keeps independently from VDI

rl1..rl0: select range limit

r1	r0	range（fres）
0	0	No restriction
0	1	+15/-16
1	0	+7/-8
1	1	+3-4

st: st goes hi will store offset into output register

fi: Enable AFC hi accuracy mode

oe: Enable AFC output register

en: Enable AFC funcition

9. Data Filter Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	al	ml	1	s1	s0	f2	f1	f0	C42Ch

al: Enable clock recovery auto-lock

ml: Enable clock recovery fast mode

s1..s0: select data filter type

s1	s0	Filter type
0	0	OOK
0	1	Digital filter
1	0	reserved

f1..f0: Set DQD threshold

10. Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	cs	r6	r5	r4	r3	r2	r1	r0	C823h

r7..r0: Set data rate

BR=10000000/29/（R+1）/（1+cs*7）

11. Output and FIFO mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	f3	f2	f1	f0	s1	s0	ff	fe	CE85h

f3..f0: Set FIFO interrupt level

s1..s0: select FIFO fill start condition

s1	s0	
0	0	VDI
0	1	Sync-word
1	0	VDI & Sync-word
1	1	Always

ff: Enable FIFO fill

fe: Enable FIFO function

12. Status Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-

This command starts with a 0 and be used to read internal status register