SAMSUNG ELECTRONICS

Product Information

ISSUE DATE : 01-09-29
MODEL : LTS180S1-HF1

Note : This product information is subjet to change after 3 months of issue date.

PREPARED BY : AMLCD Technical Customer Service Team

Samsung Electronics Co . , LTD.

Contents

Revision History

Data	Rev. No.	Page	Summary
May.15. 2001	000		Rev.000 was issued.
June.11. 2001	001	14	Input Signal & Power were changed.
Aug.17. 2001	002		TBD items were defined.
Sep.29. 2001	003	8	Optical Characteristics were fixed.
		12	Power Dissipations were fixed.
			* Stand-by: 0.15mW, Still: 8mW, Full: 10mW max
		26~27	Power On/Off Sequence was defined.
		28	Initializing Sequence was defined.
		29	Stand-by / Wake-up Sequence was defined.

General Description

*** Description**

LTS180S1-HF1 is a transmissive type color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching devices. This model is composed of a TFT-LCD module, a driver circuit and a back-light unit. The resolution of a 1.8" contains 128 x 160 pixels and can display up to 4,096 colors.

*** Features**

- Transmissive type and Back-Light with three LEDs are available.
- TN(Twisted Nematic) mode.
- Line inversion mode.
- i80 series 8bit parallel interface with on-chip display RAM.
- Stand-by, Partial, Still and Full mode are available.
- Low Power consumption.

*** Applications**

- Display terminals for HHP application products.

*** General information**

Items	Specification	Unit	Note
Display area	28.032(H) x 35.04(V)	mm	-
Driver element	a-Si TFT active matrix	-	-
Display colors	4,096	colors	-
Number of pixels	128(H) x 160(V)	pixel	-
Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.219(H) x 0.219(V)	mm	-
Display mode	Normally White	-	-
Viewing direction	12	o'clock	-
Surface Treatment	3	H	-

*** Mechanical information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	36.06	36.26	36.46	mm	-
	Vertical(V)	46.01	46.21	46.41	mm	(1)
	Depth(D)	3.36	3.51	3.66	mm	(1)
Weight		-	11	12	g	-

Note (1) Without FPC

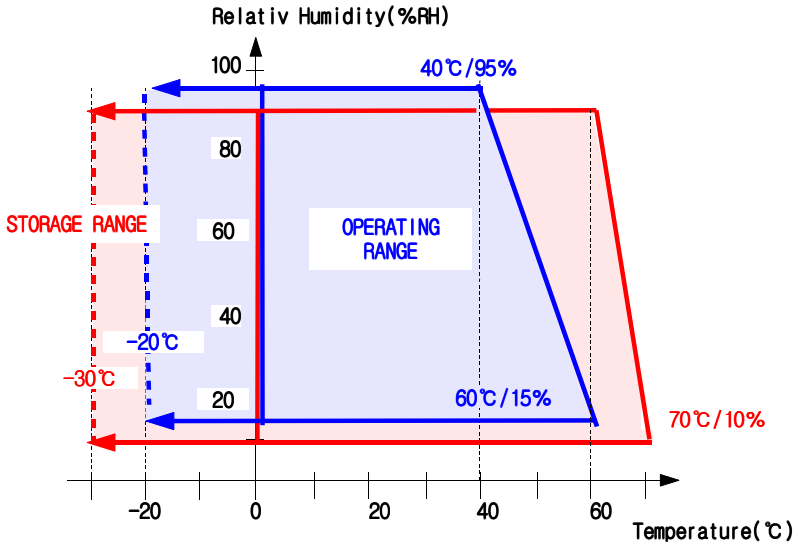
Refer to the Outline Dimension in the page 30 for further information.

1. Absolute Maximum Ratings

1.1 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Note
Storage temperature	T_{STG}	-30	70	℃	(1)
Operating temperature (Ambient temperature)	T_{OPR}	-20	60	℃	(1),(2)

Note (1) 95 % RH Max. (40 °C ≥ Ta)
Maximum wet-bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation.



(2) In case of below 0° , the response time of liquid crystal (LC) becomes slower and the color of panel becomes darker than normal one.
Level of retardation depends on temperature, because of LC's characteristics.

1.2 Electrical Absolute Ratings

(1) TFT-LCD Module

(Ta = 25 ± 2°C, V_{SS}=GND=0)

Characteristics	Symbol	Min.	Max.	Unit	Note
Logic supply voltage	V_{DDI}	-0.5	6.5	V	-
I/O buffer voltage	V_{DD}	-0.5	V_{DDI}+0.5	V	-

(2) Back-Light Unit

(Ta = 25 ± 2°C)

Item	Symbol	Min.	Max.	Unit.	Note
Current	I_B	-	25	mA	(1)

Note (1) Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded.
Functional operation should be restricted to the conditions described under normal operating conditions.

2. Optical Characteristics

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (1).
Measuring equipment: BM-5A, BM-7, PR-650, EZ-Contrast

(Ta = 25 ± 2°C, V_{DDI} = V_{DD} = 2.7V, I_B = 15mA)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast ration (Test point ③)		C/R	NOTE (1) $\phi = 0$ $\theta = 0$ Normal Viewing Angle	130	150	-	-	(2) BM-5A
Luminance of white (Test point ③)		Y_L		120	150	-	cd/m2	(3) BM-5A
Response time	Rising:Tr	Tr+Tf		-	25	30	msec	(4) BM-7
	Falling:Tf							
Color chromaticity (CIE 1931)	White	Wx		0.2159	0.3159	0.4159	-	(5) PR-650
		Wy		0.2550	0.3550	0.4550		
	Red	Rx		0.3869	0.4869	0.5869		
		Ry		0.2666	0.3666	0.4666		
	Green	Gx		0.2259	0.3259	0.4259		
		Gy		0.3626	0.4626	0.5626		
	Blue	Bx		0.0607	0.1607	0.2607		
		By		0.1118	0.2118	0.3118		
Viewing angle	Hor.	θL	C/R≥10	50	-	-	Degrees	(6) Ez-Contrast
		θR		50	-	-		
	Ver.	ϕH		50	-	-		
		ϕL		20	-	-		
Flicker		F	I_B = 15mA	-	-	3.5	%	(7) BM-7

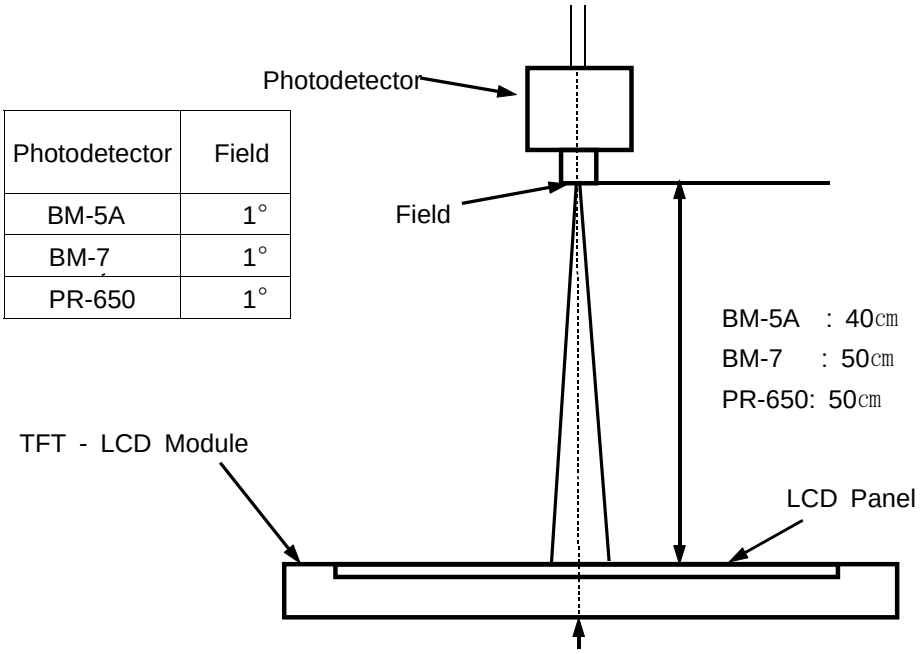
Note (1) Test Equipment Setup

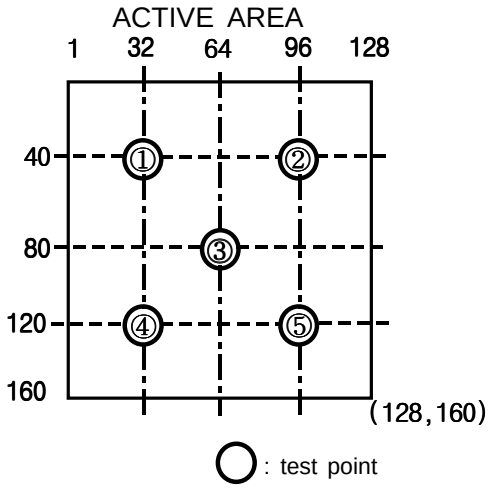
After stabilizing and leaving the panel alone at a given temperature for 30 min , the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. 30 min after lighting the back-light. This should be measured in the center of screen.

Back-Light current : 15mA

Environment condition : Ta = 25 ± 2 °C

Photodetector	Field
BM-5A	1°
BM-7	1°
PR-650	1°





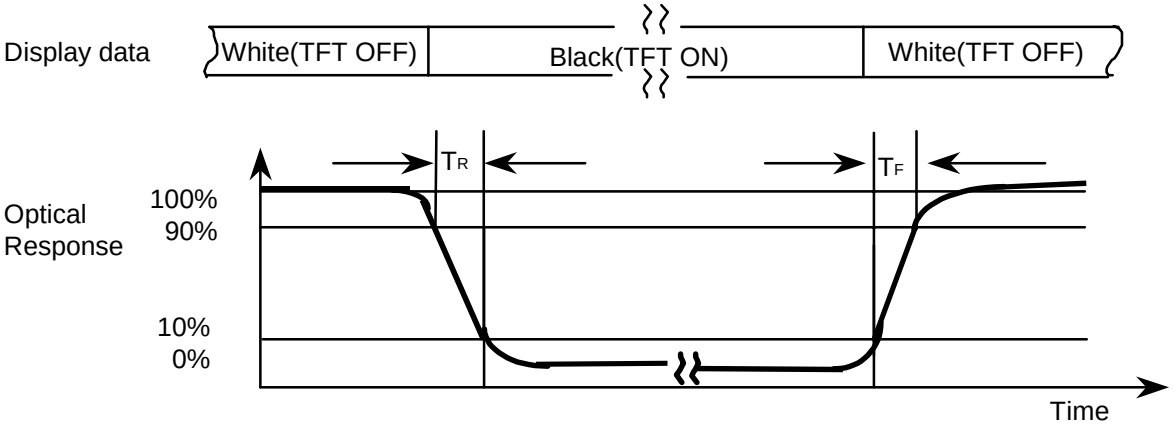
Note (2) Definition of Contrast Ratio (C/R) : Ratio of gray max (Gmax) & gray min (Gmin) at the test point ③

$$CR = \frac{G\max}{G\min}$$

* Gmax : Luminance with all pixels white
* Gmin : Luminance with all pixels black

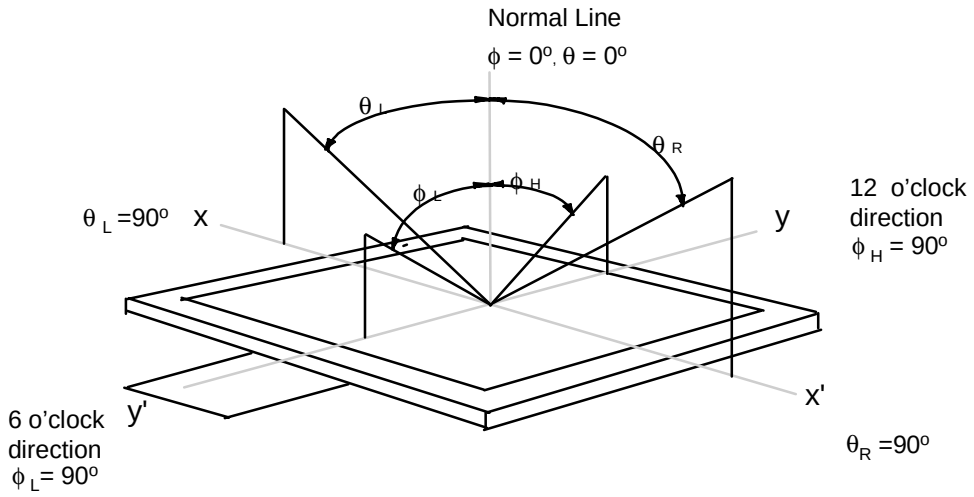
Note (3) Definition of Luminance of White : Luminance of white at the test point ③

Note (4) Definition of Response time : Sum of Tr ,Tf



Note (5) Definition of Color Chromaticity (CIE 1931)
Color coordinate of white & red, green, blue at center point.

Note (6) Definition of Viewing Angle : Viewing angle range (CR≥ 10)



Note (7) Definition of Flicker level

$$F = \frac{FlicKer\_Voltage\_pp}{LMD\_Voltage\_dc} * 100\%$$

One maximum value of three estimated values

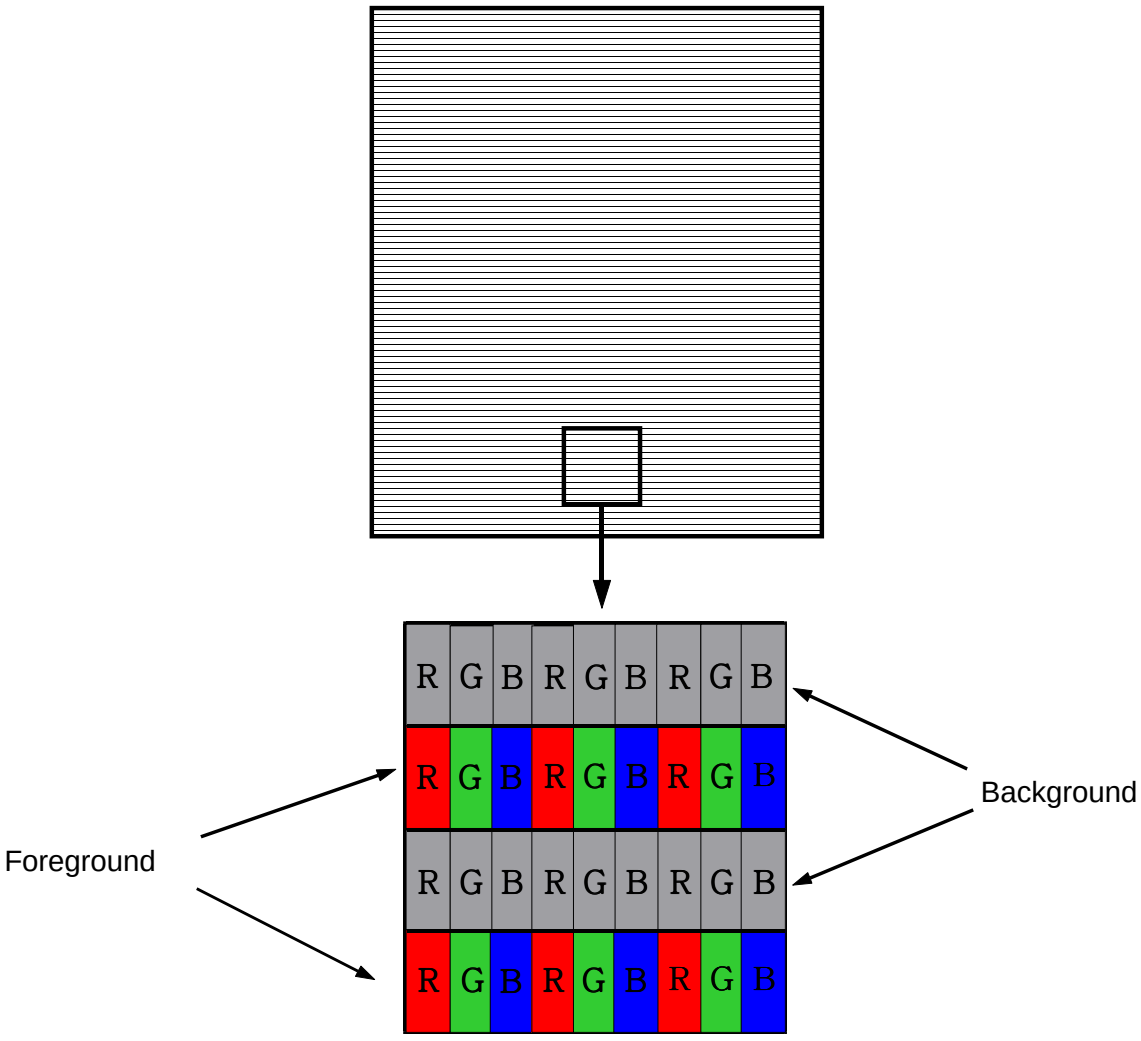
For this test, an LMD(Light Measurement Device) is needed with adequate response time to track any visible rate flicker component and with a voltage level output proportional to luminance intensity .

Back-light current : I_B = 15mA

Measurement distance : 50cm

Test Point : Test Point ③

Test Pattern : Horizontal stripe pattern



3. Electrical Characteristics

3.1 TFT-LCD Module

Ta = 25 ± 2°C

Characteristics		Symbol	Min.	Typ.	Max.	Unit	Note
Digital supply voltage		V_{DDI}	2.5	2.7	3.6	V	-
I/O buffer voltage		V_{DD}	1.8	-	V_{DDI}	V	-
Power Dissipation	Stand-by	P_{St}	-	-	0.15	mW	(1),(2)
	Still	P_S	-	-	8		(1)
	Full	P_F	-	-	10		
Frame frequency		f_{Frame}	60.7	65	120	Hz	(4)

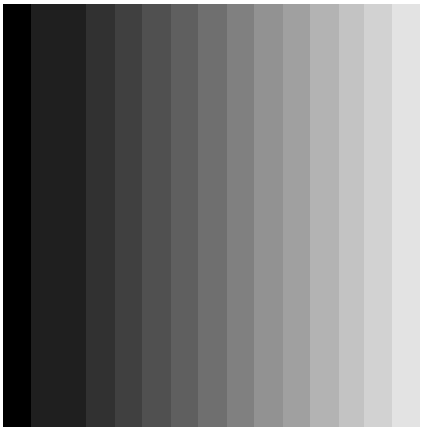
* To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the Chapter 10. Power On/Off Sequence.

Note (1) V_{DD} = V_{DDI} = 2.7V, f_{Frame} = 65 Hz

(2) Refer to the Chapter 12. Stnad-by/Wake-up Sequence.

(3) Power dissipation check pattern

▶ 16 Gray Vertical Stripe Pattern



(4) Uncalibrated condition

For calibration, refer to the Chapter 6.3 Frame Frequency Calibration

3.2 Back-Light unit

The back-light system is an edge-lighting type with three white LED(Light Emitting Diode)s.

(Ta=25 ± 2°C)

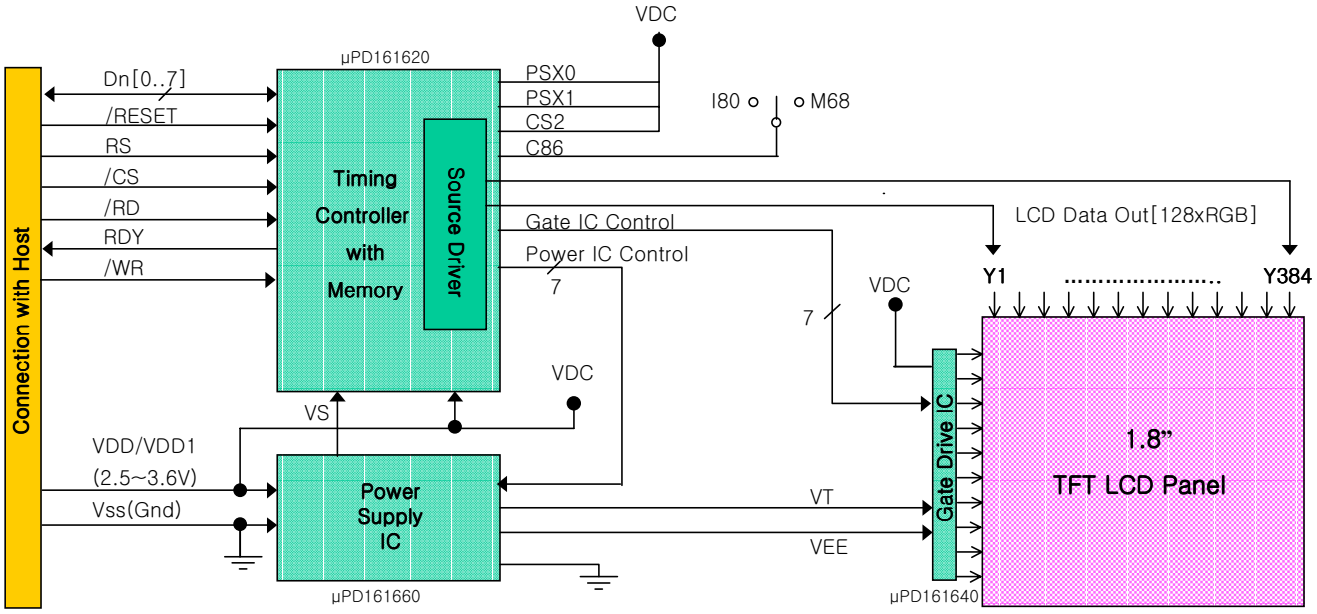
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Current	I_B	-	15	20	mA	(1)
Power Consumption	P_{BL}	-	144	-	mW	(2)

Note (1) Three LEDs serial type. V_B=9.6± 0.7V

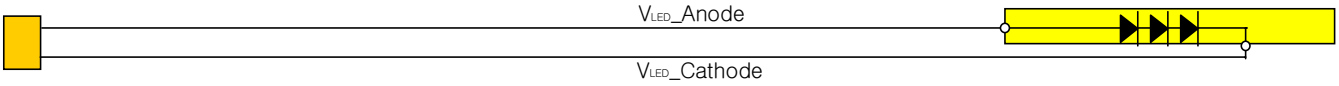
(2) Refer to I_B x V_B to calculate. V_B=9.6± 0.7V

4. Block Diagram

4.1 TFT-LCD Module (Interface System Structure)



4.2 Back-light Unit



5. Input Terminal Pin Assignment

5.1 Input Signal & Power (Connector : 20Pin FPC Hot-Bar type)

Pin No	Symbol	Description	Input/Output	Note
1	NC	No Connection	-	-
2	GND	Power Ground	-	-
3	GND	Power Ground	-	-
4	/RD	Memory Read Enable	Input	(1)
5	/WR	Memory Write Enable	Input	(2)
6	RS	Index Register/ Data,Command	Input	(3)
7	D0	Data 0	Input/Output	(4)
8	D1	Data 1		
9	D2	Data 2		
10	D3	Data 3		
11	D4	Data 4		
12	D5	Data 5		
13	D6	Data 6		
14	D7	Data 7		
15	/CS	Chip Select	Input	(5)
16	/RESET	System Reset	Input	(6)
17	RDY	Ready	Output	(7)
18	V_{DDI}	Logic Supply Voltage	-	-
19	V_{DD}	I/O Buffer Voltage	-	-
20	NC	No Connection	-	-

Note (1) Data is output to the data bus only when this pin is low.

(2) Data is written at the rising edge of this signal.

(3) Usually, this pin is connected to the LSB of the standard CPU address bus and is used to distinguish between data from index registers and data/commands.
RS=H: Indicates that data from D0 to D7 is data/command
RS=L: Indicates that data from D0 to D7 is index register contents

(4) These pins comprise 8-bit bi-directional data.
When the chip is not selected, D0 to D7 are in high impedance mode.

(5) This pin is used for chip select signal. When /CS=L, the chip is active and can perform data input/output operations including command and data I/O.

(6) When /RESET is low, an internal reset is performed. The reset operation is executed at the /RESET signal level. Be sure to perform reset via this pin at power application.

(7) This pin is the ready signal output. This pin connects to external WAIT pin in CPU.

5.2 Back-Light Unit (Connector : 2Pin FPC Solder type)

Pin No.	Symbol	Fucnction
1	Anode	LED Input Terminal
2	Cathode	GND

5.3 Input Signal,Basic Display Colors and Gray Scale of Each Colors

COLOR	DISPLAY	DATA SIGNAL												GRAY SCALE LEVEL
		RED				GREEN				BLUE				
		R0	R1	R2	R3	G0	G1	G2	G3	B0	B1	B2	B3	
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	-
	BLUE	0	0	0	0	0	0	0	0	1	1	1	1	-
	GREEN	0	0	0	0	1	1	1	1	0	0	0	0	-
	CYAN	0	0	0	0	1	1	1	1	1	1	1	1	-
	RED	1	1	1	1	0	0	0	0	0	0	0	0	-
	MAGENTA	1	1	1	1	0	0	0	0	1	1	1	1	-
	YELLOW	1	1	1	1	1	1	1	1	0	0	0	0	-
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	-
GRAY SCALE OF RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	R0
	DARK	1	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	R2
		:	:	:	:	:	:	:	:	:	:	:	:	R3~R12
		:	:	:	:	:	:	:	:	:	:	:	:	
		1	0	1	1	0	0	0	0	0	0	0	0	R13
	↓	0	1	1	1	0	0	0	0	0	0	0	0	R14
	LIGHT													
	RED	1	1	1	1	0	0	0	0	0	0	0	0	R15
GRAY SCALE OF GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	G0
	DARK	0	0	0	0	1	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	1	0	0	0	0	0	0	G2
		:	:	:	:	:	:	:	:	:	:	:	:	G3~G12
		:	:	:	:	:	:	:	:	:	:	:	:	
		0	0	0	0	1	0	1	1	0	0	0	0	G13
	↓	0	0	0	0	0	1	1	1	0	0	0	0	G14
	LIGHT													
	GREEN	0	0	0	0	1	1	1	1	0	0	0	0	G15
GRAY SCALE OF BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	B0
	DARK	0	0	0	0	0	0	0	0	1	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	1	0	0	B2
		:	:	:	:	:	:	:	:	:	:	:	:	B3~B12
		:	:	:	:	:	:	:	:	:	:	:	:	
		0	0	0	0	0	0	0	0	1	0	1	1	B13
	↓	0	0	0	0	0	0	0	0	0	1	1	1	B14
	LIGHT													
	BLUE	0	0	0	0	0	0	0	0	1	1	1	1	B15

Note) Definition of Gray :

Rn : Red Gray, Gn : Green Gray, Bn : Blue Gray (n = Gray level)

Input Signal : 0 = Low level voltage, 1 = High level voltage

※R3,G3,B3:MSB, R0,G0,B0:LSB

6. Description of Functions

(For more details, refer to the Appendix 1: μ PD161620 IC Specification)

6.1 Selection of data transfer mode

Two modes are available for transferring data to the display RAM. The mode is selected according to the setting of the DXT command, as shown below.

(1) 1-pixel/2-byte mode (DXT=1)

Data bus side

1st byte								2nd byte							
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
Dot1				Dot2				Dot3				Invalid data			
1st pixel															

Display RAM side

(2) 2-pixel/3byte mode (DXT=0)

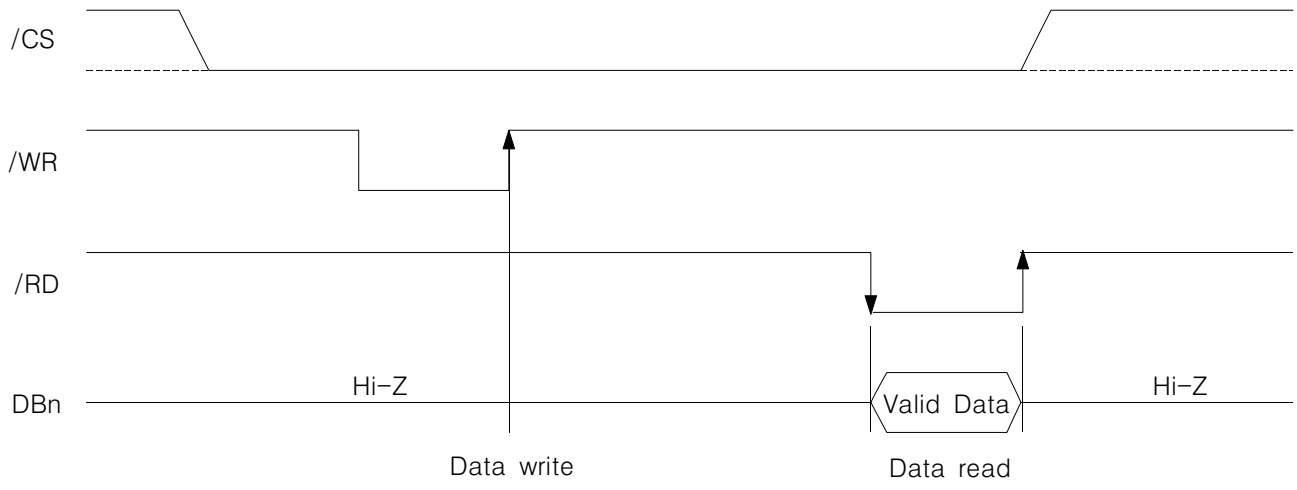
Data bus side

1st byte								2nd byte								3rd byte							
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D9	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D9
Dot1				Dot2				Dot3				Dot1				Dot2				Dot3			
1st pixel												2nd pixel											

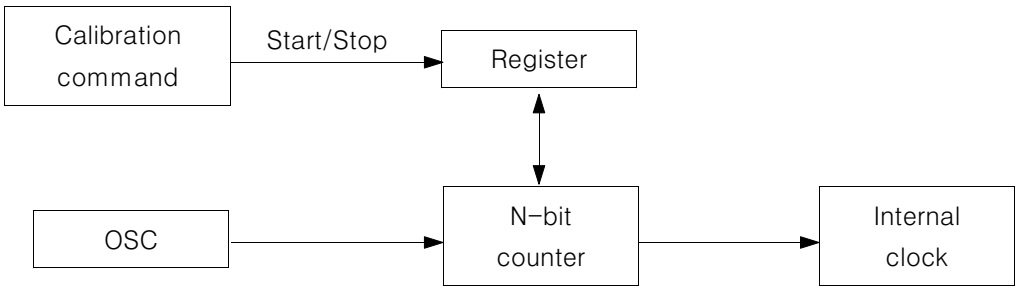
Display RAM side

6.2 Interface Data Bus Status



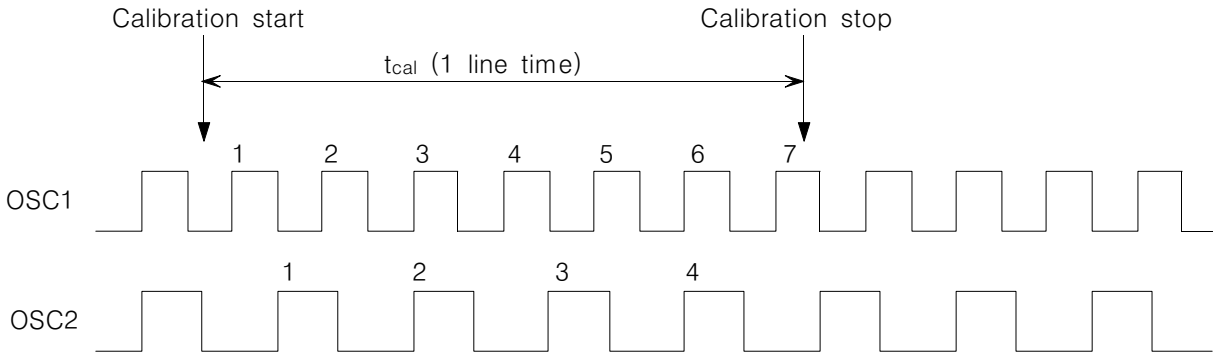
6.3 Frame Frequency Calibration

The time to select one line is set by the calibration start and stop commands.



The calibration function involves counting the number of oscillation clocks generated between the start and stop signals and storing that number in a register. The number of oscillation clocks is then continually compared with this register value in subsequent operations, and the time of the clock number stored in the register is set as 1 line selection time, and used as the internal reference clock.

Using this function allows the frame frequency to be held at a constant value, even when the oscillation frequency is irregular.



$t_{cal} = 1/(f_{Frame} \times 177)$

f_{Frame} = Frame frequency

n: Line numbers

7. Reset

If the /RESET input becomes L or the reset command is input, the internal timing generator is initialized. The reset command will also initialize each register to its default value. These default values are listed in the table below.

Register		/RESET Pin	Reset Command	Default Value	Note
Index registor	IR	X	O	00H	-
Control register1	R0	X	O	00H	-
Control register2	R1	X	O	00H	-
X address register	R3	X	O	00H	-
Y address register	R5	X	O	00H	-
Reverse setting register	R6	X	O	00H	-
Display memory	R11	X	X	–	(2)
Scroll area start line register	R22	X	O	00H	-
Scroll area line count register	R24	X	O	00H	-
Scroll step count register	R26	X	O	00H	-
Partial off area color register	R27	X	O	00H	-
Partial 1display area start line register	R28	X	O	00H	-
Partial 2display area start line register	R29	X	O	00H	-
Partial 1display area line register	R30	X	O	00H	-
Partial 2display area line register	R31	X	O	00H	-
Power supply control register1	R32	X	O	00H	-
Power supply control register2	R34	X	O	00H	-
Calibration register	R38	X	O	00H	(3)
Output port register	R42	X	O	00H	-
Input port register	R43	X	O	00H	-
Test mode	R44 to R47	X	O	00H	-

O: Default value set, X: Default value not set

Note (1) The internal counters are initialized only by reset from the /RESET pin. Be sure to perform reset via the /RESET pin at power application.

(2) The contents of RAM are saved in the case of both reset by /RESET pin and reset by reset command. Note that the RAM contents are undefined immediately after the power is turned on.

(3) The following value is set as the calibration setting time, t_{cal}, in a reset by reset command.

$t_{cal} = 1/f_{osc} \times 32$

8. Command

8.1 Command List

	Index Register						Register Name		R/W	Data							
	5	4	3	2	1	0				7	6	5	4	3	2	1	0
1st byte	0	0	0	0	0	0	IR	Index register	W			IR5	IR4	IR3	IR2	IR1	IR0
	0	0	0	0	0	0	R0	Control register 1	R/W	RMW	DISP	STBY			ADX	ADC	ADR
	0	0	0	0	0	1	R1	Control register 2	R/W	FDM		DTX	LPM	GSM	COLOR	DTY	INC
	0	0	0	0	1	0	R2	Reset	W								CRES
	0	0	0	0	1	1	R3	X address register	R/W	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0
	0	0	0	1	0	0	R4										
	0	0	0	1	0	1	R5	Y address register	R/W	YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0
	0	0	0	1	1	0	R6	Reverse setting register	R/W								INV
	0	0	0	1	1	1	R7										
	0	0	1	0	0	0	R8										
	0	0	1	0	0	1	R9										
	0	0	1	0	1	0	R10										
	0	0	1	0	1	1	R11	Display memory	R/W	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	1	1	0	0	R12										
	0	0	1	1	0	1	R13										
	~						~	~	~	~							
	0	1	0	1	0	0	R20										
	0	1	0	1	0	1	R21										
	0	1	0	1	1	0	R22	Scroll area start line register	R/W	SSL7	SSL6	SSL5	SSL4	SSL3	SSL2	SSL1	SSL0
	0	1	0	1	1	1	R23										
	0	1	1	0	0	0	R24	Scroll area line count register	R/W	SAW7	SAW6	SAW5	SAW4	SAW3	SAW2	SAW1	SAW0
	0	1	1	0	0	1	R25										
	0	1	1	0	1	0	R26	Scroll step count register	R/W	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0
	0	1	1	0	1	1	R27	Partial off area color register	R/W						PGD2	PGD1	PGD0
2nd	0	1	1	1	0	0	R28	Partial 1 display area start line register	R/W	P1SL7	P1SL6	P1SL5	P1SL4	P1SL3	P1SL2	P1SL1	P1SL0
byte	0	1	1	1	0	1	R29	Partial 2 display area start line register	R/W	P2SL7	P2SL6	P2SL5	P2SL4	P2SL3	P2SL2	P2SL1	P2SL0
	0	1	1	1	1	0	R30	Partial 1 display area line count register	R/W	P1AW7	P1AW6	P1AW5	P1AW4	P1AW3	P1AW2	P1AW1	P1AW0
	0	1	1	1	1	1	R31	Partial 2 display area line count register	R/W	P2AW7	P2AW6	P2AW5	P2AW4	P2AW3	P2AW2	P2AW1	P2AW0
	1	0	0	0	0	0	R32	Power supply control register 1	R/W		BGRS	VCE	VCD2	PVCOM	RGONG	RGONP	DCON
	1	0	0	0	0	1	R33										
	1	0	0	0	1	0	R34	Power supply control register 2	R/W					VCD12	VCD11		
	1	0	0	0	1	1	R35										
	1	0	0	1	0	0	R36										
	1	0	0	1	0	1	R37										
	1	0	0	1	1	0	R38	Calibration register	R/W								OC
	1	0	0	1	1	1	R39										
	1	0	1	0	0	0	R40										
	1	0	1	0	0	1	R41										
	1	0	1	0	1	0	R42	Output port register	W					OP3	OP2	OP1	OP0
	1	0	1	0	1	1	R43	Input port register	R					IP3	IP2	IP1	IP0
	1	0	1	1	0	0	R44	Test mode	R/W								
	1	0	1	1	0	1	R45	Test mode	R/W								
	1	0	1	1	1	0	R46	Test mode	R/W								
	1	0	1	1	1	1	R47	Test mode	R/W								
	1	1	0	0	0	0	R48										
	1	1	0	0	0	1	R49										
	~						~	~	~	~							
	1	1	1	1	1	0	R62										
	1	1	1	1	1	1	R63										

: Thses registers cannot be used.

8.2 Command Explanation

Register	Bit	Symbol	Function
R0	D_7	RMW	0: Address is incremented by one each time a display data read or write 1: Read modify write mode (address is incremented by one each time a display data write only)
	D_6	DISP	0: Display off (All output pins are Vss level, OSC and DC/DC converter are working) 1: Display on
	D_5	STBY	0: Normal operation 1: Stand-by function (Display read off from RAM, stop both OSC and VCOM, display off=entire data is output as 1)
	D_2	ADX	X address direction
	D_1	ADC	Column address direction
	D_0	ADR	Row address direction
R1	D_7	FDM	0: Normal operation 1: RAM data is ignored an the entire data is output as 0.
	D_5	DTX	0: 2-pixel/3-byte 1: 1-pixel/2-byte
	D_4	LPM	0: Normal 1: Low power mode
	D_3	GSM	0: Normal 1: Gate scanning stop for partial non-display area
	D_2	COLOR	0: 4096-color mode (12 bits/pixels) 1: 8-color mode (3 bits/pixels)
	D_1	DTY	0: Normal display mode 1: Partial display mode
	D_0	INC	0: X address increment 1: Y address increment
R2	D_0	CRES	0: Normal operation 1: Command reset
R3	D_7 to D_0	XA_7 to XA_0	X address register (00H to 8FH)
R5	D_7 to D_0	YA_n	Y address register (00H to AFH)
R6	D_0	INV	0: Line inversion 1: Frame inversion
R11	D_7 to D_0	D_n	Display memory (Parallel mode only)
R22	D_7 to D_0	SSL_n	Scroll area start line register (00H to AFH)
R24	D_7 to D_0	SAW_n	Scroll area line count register (00H to AFH)
R26	D_7 to D_0	SST_n	Scroll step count register (00H to AFH), invalid in partial displya mode
R27	D_7 to D_0	PGD_n	Partial off area color register (000H to 111H)
R28	D_7 to D_0	$P1SL_n$	Partial 1 display area start line register (00H to AFH)
R29	D_7 to D_0	$P2SL_n$	Partial 2 display area start line register (00H to AFH)
R30	D_7 to D_0	$P1AW_n$	Partial 1 display area line count register (00H to AFH)
R31	D_7 to D_0	$P2AW_n$	Partial 2 display area line count register (00H to AFH)

Register	Bit	Symbol	Function
R32	D_6	BGRS	0: The internal power-supply is selected as the VCOM power supply 1: Input from the external power-supply BGRIN is selected as the BCOM power supply
	D_5	VCE	0: The Vo high-level booster voltage level is V_{DD1} minus 1 level 1: The Vo high-level booster voltage level is the same level as V_{DD1}
	D_4	VCD2	0: $V_{DD2} = V_{DC} \times 2$ 1: $V_{DD2} = V_{DC} \times 3$
	D_3	PVCOM	0: VCOM power supply is V_{CC1} 1: VCOM power supply is V_S
	D_2	RGONG	0: Regulators of gate driver (V_B) are off 1: Regulators of gate driver (V_B) are on
	D_1	RGONP	0: Regulators of power supply IC (V_T,V_S) are off 1: Regulators of power supply IC (V_T,V_S) are on
	D_0	DCON	0: DC/DC converter is off 1: DC/DC converter is on
R34	D_3, D_2	VCD12, VCD11	VCD12,VCD11 = 0, 0: $V_{DD1} = V_{DC} \times 4$ = 0, 1: $V_{DD1} = V_{DC} \times 5$ = 1, 0: $V_{DD1} = V_{DC} \times 6$ = 1, 1: $V_{DD1} = V_{DC} \times 7$
R38	D_0	OC	0: Calibration start 1: Calibration stop
R42	D_3 to D_0	OP_n	Output port write
R43	D_3 to D_0	IP_n	Input port read
R44	–	–	Test mode (for IC testing only)
R45	–	–	
R46	–	–	
R47	–	–	

9. Interface Timing

(For more details, refer to the Appendix 1: μ PD161620 IC Specification)

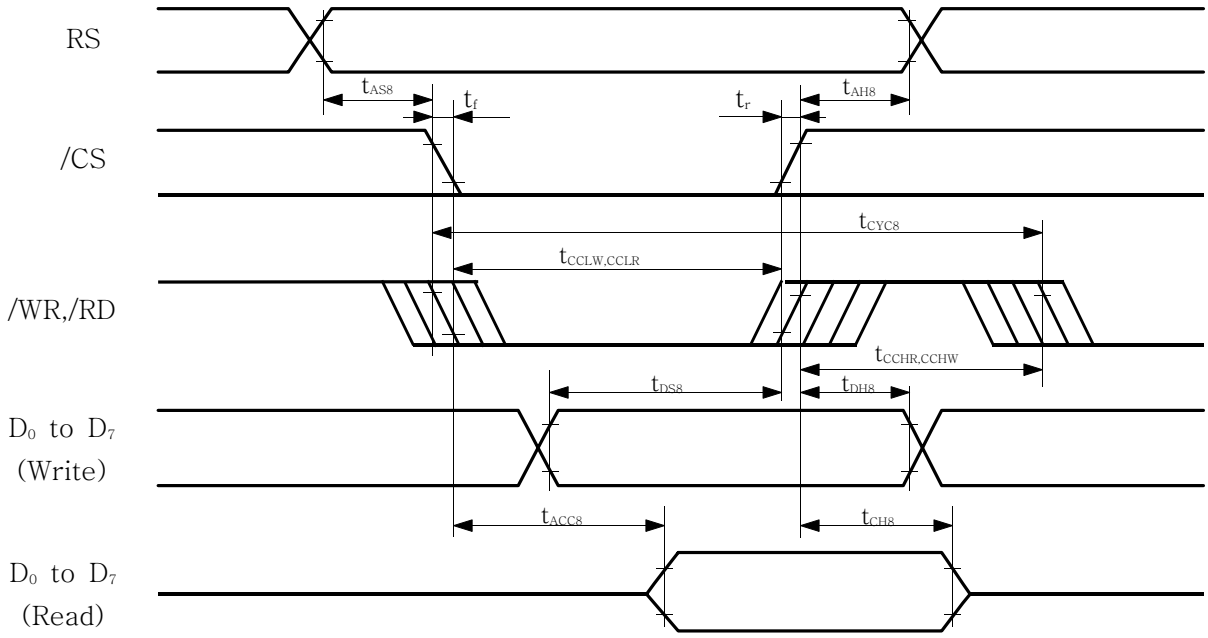
9.1 Electrical Specifications

(Ta = -30 to + 70°C, V_{DDI} = 2.5 to 3.6V, V_{DD} = 1.8V to V_{DDI})

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH1}	V_{DDI}	$0.8V_{DDI}$	-	-	V
	V_{IH2}	V_{DD}	$0.8V_{DD}$	-	-	
Low level input voltage	V_{IL1}	V_{DDI}	-	-	$0.2V_{DDI}$	
	V_{IL2}	V_{DD}	-	-	$0.2V_{DD}$	

9.2 AC Characteristics

(Ta = -30 to + 70°C, V_{DDI} = 2.5 to 3.6V, V_{DD} = 1.8V to V_{DDI})



When V_{DDI} = 2.5 to 3.6V, V_{DD} = 2.5 to 3.6V, $V_{DDI} \geq V_{DD}$

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		250			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	120			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	140			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	60			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	80			ns
Data setup time	t_{DS8}	D_0 to D_7	80			ns
Data hold time	t_{DH8}	D_0 to D_7	5			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100pF			140	ns
Output disable time	t_{OH8}	D_0 to D_7, C_L = 100pF	10		140	ns

When V_{DDI} = 2.5 to 3.6V, V_{DD} = 1.8 to 2.5V, $V_{DDI} \geq V_{DD}$

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Address hold time	t_{AH8}	RS	0			ns
Address setup time	t_{AS8}	RS	0			ns
System cycle time	t_{CYC8}		333			ns
Control low-level pulse width (/WR)	t_{CCLW}	/WR	120			ns
Control low-level pulse width (/RD)	t_{CCLR}	/RD	160			ns
Control high-level pulse width (/WR)	t_{CCHW}	/WR	100			ns
Control high-level pulse width (/RD)	t_{CCHR}	/RD	140			ns
Data setup time	t_{DS8}	D_0 to D_7	100			ns
Data hold time	t_{DH8}	D_0 to D_7	5			ns
/RD access time	t_{ACC8}	D_0 to D_7, C_L = 100pF			180	ns
Output disable time	t_{OH8}	D_0 to D_7, C_L = 100pF	10		180	ns

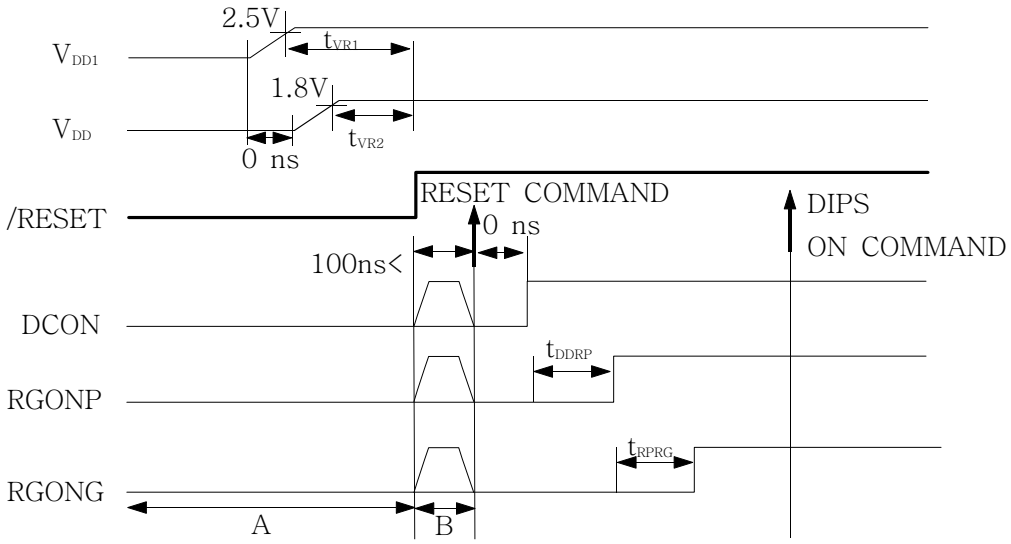
Note (1) Typ. values are reference values when Ta = 25°C

(2) The input signal's rise/fall times are rated as 15ns or less.

(3) All timing is rated based on 20 to 80% of V_{DD}

10. Power On/Off Sequence

10.1 Power On Sequence



① All two power supplies, V_{DD1}, and V_{DD} can be at the same time.

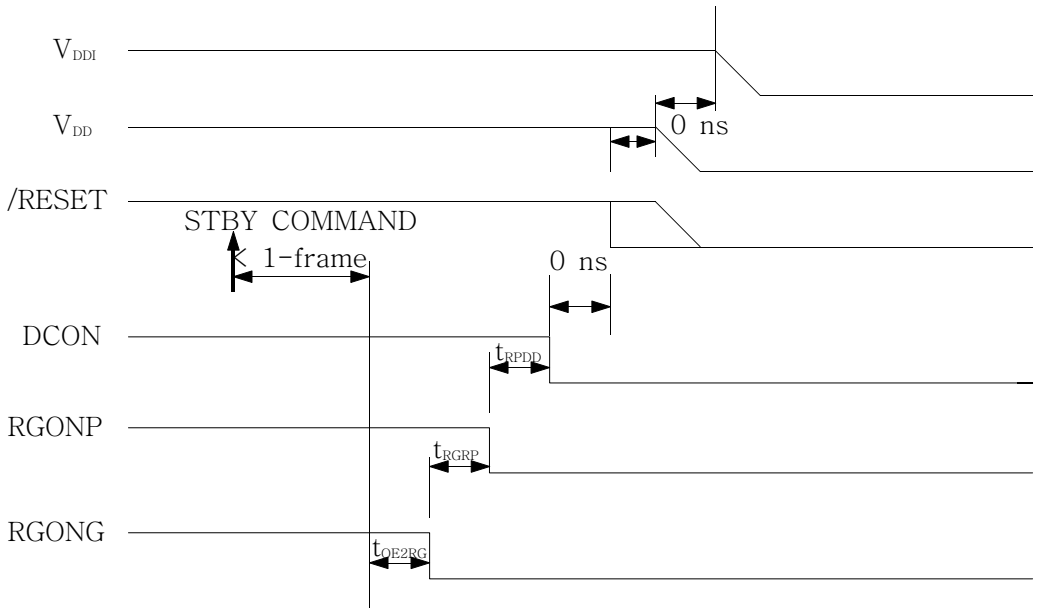
② The wait time between when the /RESET signal rises and when the RESET command is acknowledged must be at least 100ns.

③ The logical status of the DCON, RGONG, and RGONP pins in the period between when the /RESET signal rises and when the RESET command(↑part) is acknowledged (B period) is undefined. Be aware, therefore, that the gate output may be undefined and the DC/DC converter and the regulator may be on. If the B period is sufficiently short however, it is unlikely that the display will be affected. Note that the gate output MAX value in the B period must be determined separately as a specification of the LCD module.

④ The Pins are re-fixed to the following levels by the source driver when the RESET command is input. Note that the gate output is fixed to the V_B level, and the DC/DC converter and the regulators are off. DCON, RGONG, RGONP:L(low level)

⑤ Set a timing that ensures the DCON, RGONP, and RGONG pins are shifted to high level in that order after the RESET command is input. At this time, the DC/DC converter and the regulator are on. Before that, the booster level must have been set up(by BGRS, $V_{CE,}V_{CD2}$, PVCOM of R32 register and R34 register of the µPD161620). The t_{DDRP} and t_{RPRG} timing must be determined separately as specifications of the LCD module.

10.2 Power Off Sequence

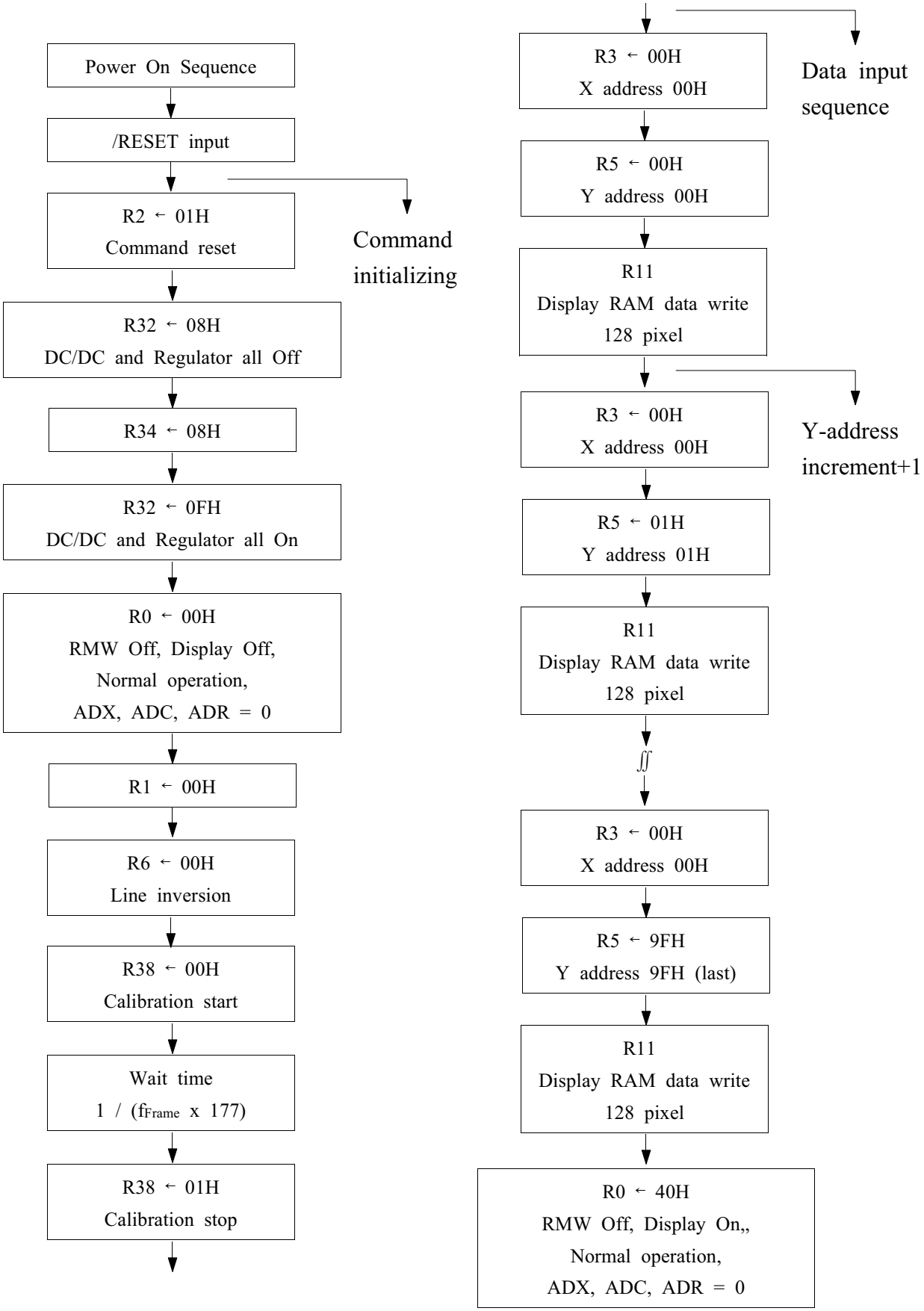


① Set a timing that ensures the RGONG, RGONP, and DCON pins are shifted to low level in that order after the panel load has been sufficiently discharged (t_{OE2RG} timing). At this time, the DC/DC converter and the regulators are off.
The $t_{OE2RG,}$ $t_{RGRP,}$ and t_{RPPD} timings must be determined separately as specifications of the LCD module.

② Although it is unnecessary to input the RESET command to the source driver, for designs in which the system is reset when the power supply is turned off,make settings that ensure /RESET=L at DCON=L and subsequent timings.

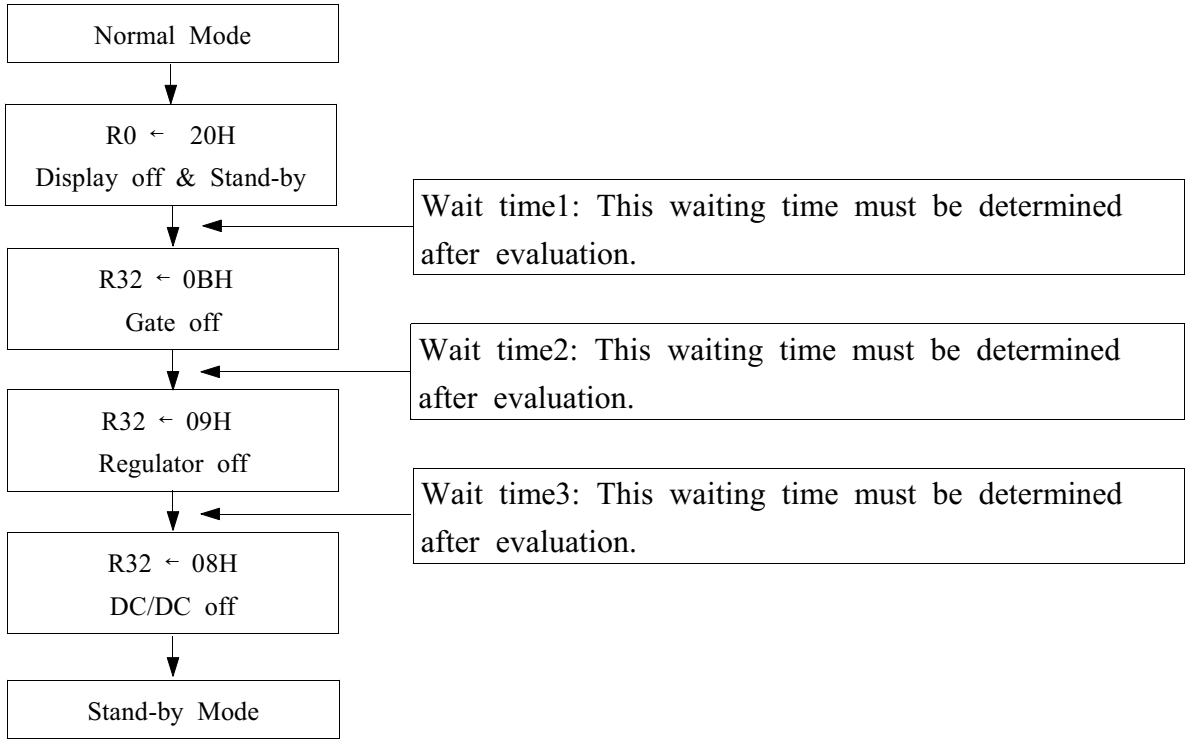
③ All two power supplies, $V_{DD1,}$ and V_{DD} can be off at the same time.

11. Initializing Sequence

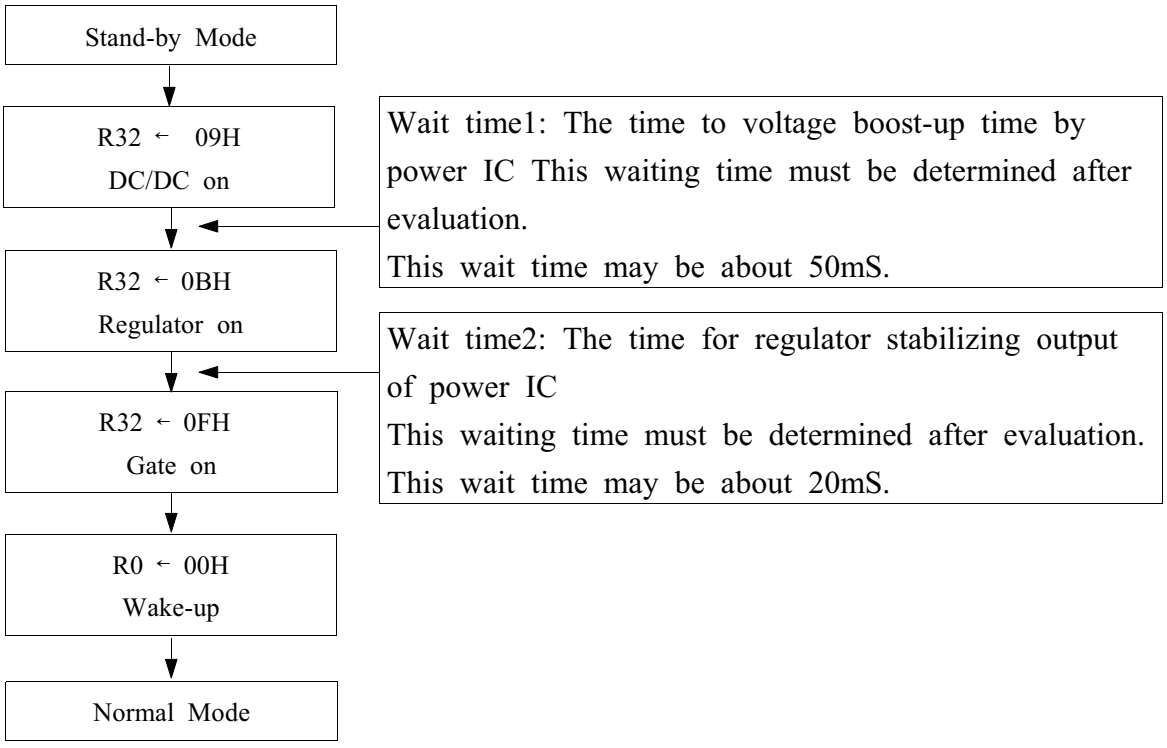


12. Stand-by / Wake-up Sequence

12.1 Stand-by Sequence



12.2 Wake-up Sequence

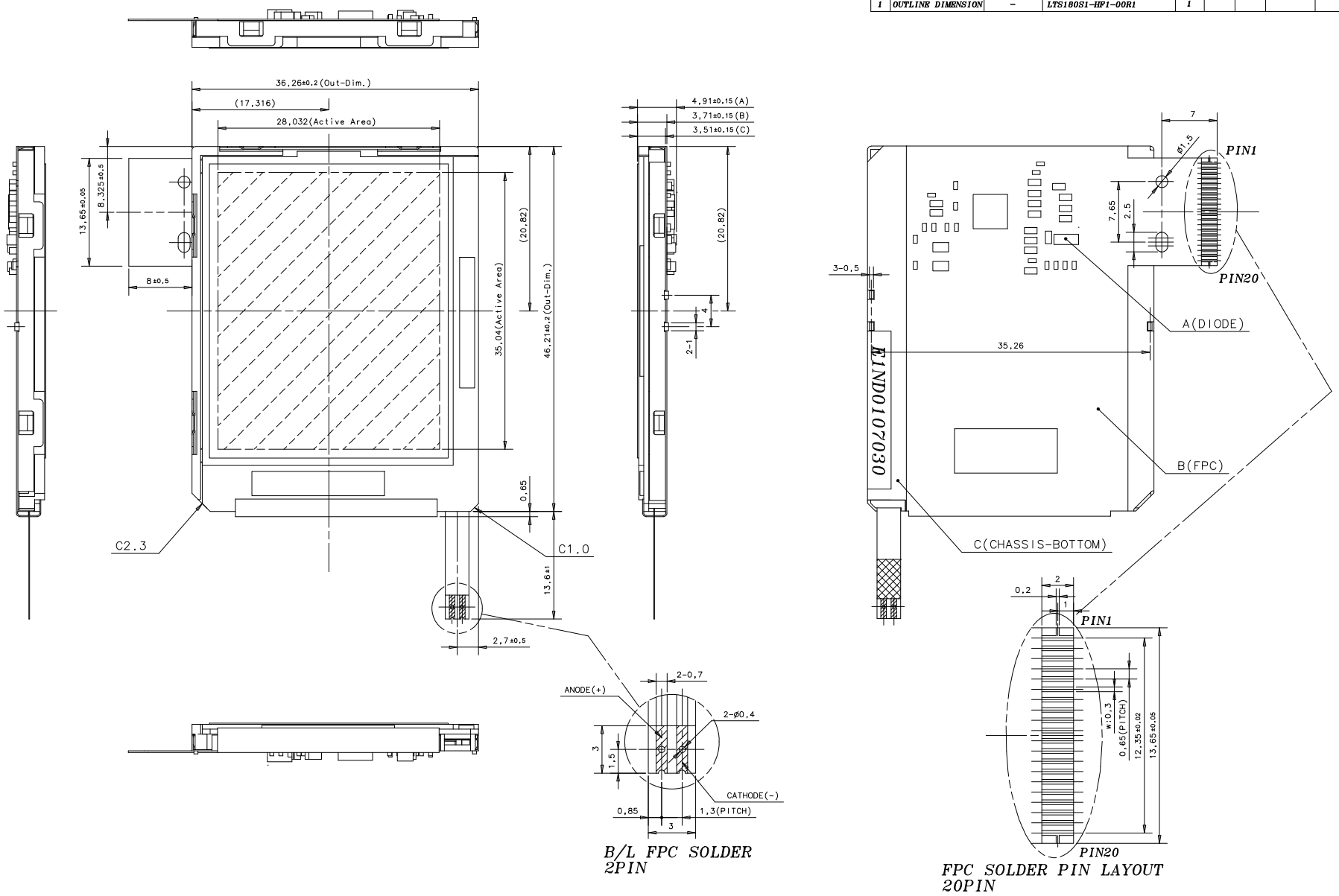


13. Outline Dimension

See the next page.

FILE NO.

NO	PART NAME	CODE NO	SPECIFICATION	Q'TY	WEIGHT FINISH	WEIGHT MATERIAL	UNFOLDED DIM. OF. MATERIAL	REMARK
1	OUTLINE DIMENSION	–	LTS180S1-HF1-00R1	1				



REVISION

GENERAL TOLERANCE			
STEP	LEVEL 1	LEVEL 2	LEVEL 3
0 < X ≤ 4	±0.05	±0.1	±0.2
4 < X ≤ 16	±0.08	±0.15	±0.3
16 < X ≤ 64	±0.12	±0.25	±0.5
64 < X ≤ 256	±0.25	±0.4	±0.8

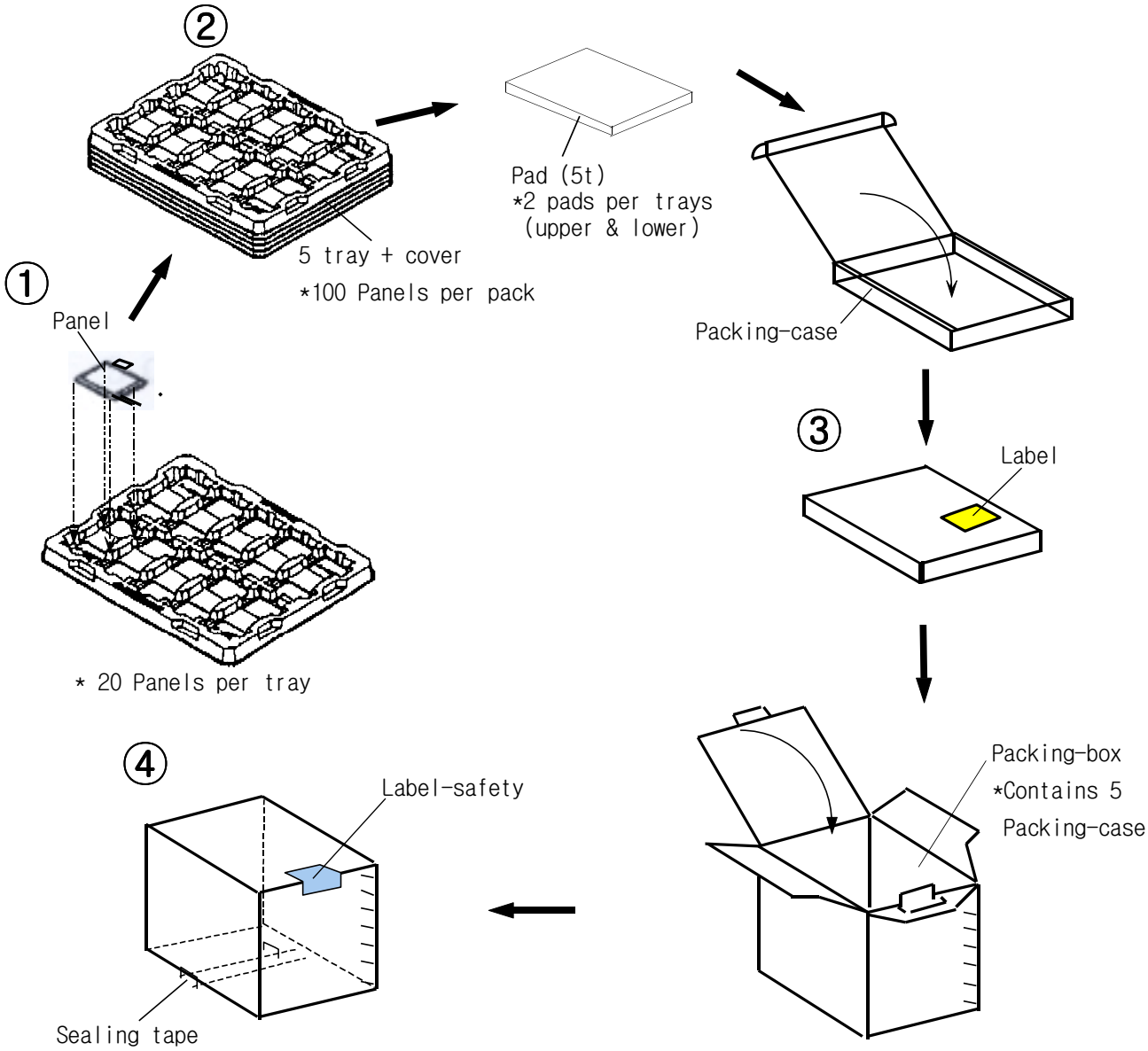
REV	DATE	DESCRIPTION OF REVISION				REASON	CHG'D BY
UNIT	mm	DRA'N BY	DES'D BY	CHK'D BY	APP'D BY		
SCALE	3 / 1	S.M.KIM	S.M.KIM	K.H.KHO	I.S.LEE		
TOLERANCE	LEVEL 2	'01. 05. 17	'01. 05. 17	'01. 05. 17	'01. 05. 17		

SAMSUNG ELECTRONICS

SPEC. NO

MODEL NAME	LTS180S1-HF1-00R1		
PART/SHEET NAME	OUTLINE DIMENSION	SHEET	1 / 1
CODE NO.	–	VER.	00

14. Packing



Note (1) Total : Case: Approx. 2.2 Kg
Box: Approx. 11.5 Kg

(2) Size : Case: 490(W) x 342(D) x 58(H)
Box: 505(W) x 355(D) x 312(H)

(3) Place the panels in the tray facing the direction shown in the figure.

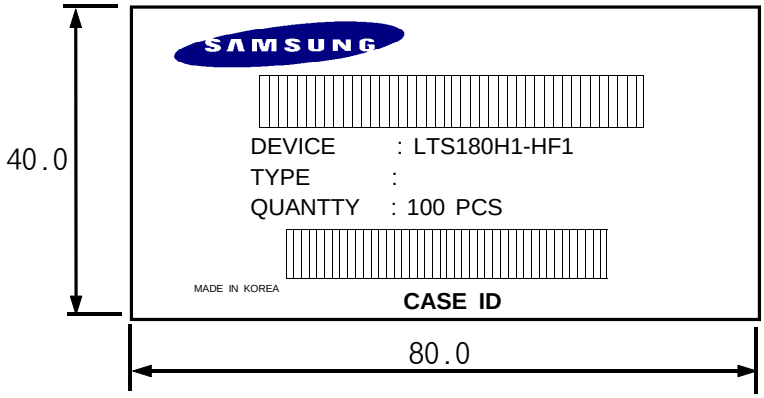
(4) Place 5 tray and cover(empty tray) and pads inside the packing-case.

(5) Place 5 packing-case inside the packing-box.(Affix the label)

(6) Seal the packing-box. Affix the label-safety.

15. MARKING & OTHERS

(1) Packing case attach



CASE ID : V 00 00 00001

- Serial No.(00001-99999)
- Week
- Year
- Device

16. General Precautions

16.1 Handling

(a) When the module is assembled, it should be attached to the system firmly. Be careful not to twist and bend the module.

(b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.

(d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(f) The desirable cleaners are water, IPA(Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth . In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(h) Protect the module from static , it may cause damage to the CMOS Gate Array IC.

(i) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(j) Do not disassemble the module.

(k) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(l) Pins of I/F connector shall not be touched directly with bare hands.

16.2 Storage

(a) Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35° C and relative humidity of less than 70%.

(b) Do not store the TFT-LCD module in direct sunlight.

(c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

16.3 Operation

(a) Do not connect, disconnect the module in the "Power On" condition.

(b) Power supply should always be turned on/off by the item 10 "Power on/off sequence"

16.4 Others

(a) The Liquid crystal is deteriorated by ultraviolet, do not leave it in direct sunlight and strong ultraviolet ray for many hours.

(b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, and so on)
Otherwise the panel may be damaged.

(d) If the panel displays the same pattern continuously for a long period of time, it can be the situation when the image "Sticks" to the screen.

(e) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.